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EXAMINER	
HIGHTER, TREVILLIAN H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,728	PARKER ET AL.	
	Examiner	Art Unit	
	TREVILLIAN HIGHTER	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/5/2007, 11/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-68 are pending in this application.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 41 has been renumbered to 51.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Modelski et al. (Patent No. US 6,665,755 B2), hereinafter Modelski.

5. With respect to claim 20, Modelski discloses a packet processor (column 5, lines 20-21), wherein the packet processor generates processing data (column 5, lines 20-30; column 3, lines 23-34) and while revising packet data based on a packet header modification recipe (column 3, lines 48-53, modifications of packet is interpreted to include packet header) and the status of one or more control structures (column 7, lines 52-55, 60-64); and a buffer (column 6, line 32; column 3, lines 23-34), wherein the buffer records the processing data (column 5, lines 21-23) and the status of the one or more control structures (column 6, lines 33-34; column 3, lines 23-34).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1, 37, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Floyd et al. (Patent No. 7,117,126 B2), hereinafter Floyd.**

8. With respect to claim 1, Modelski discloses a packet processor (column 5, lines 20-21), wherein the packet processor generates processing data (column 5, lines 20-30; column 3, lines 23-34) based on one or more control structures (column 7, lines 52-55, 60-64) while revising packet data (column 3, lines 48-53), wherein the packet processor generates the processing data while performing one or more lookup cycles (column 5, lines 20-30; column 3, lines 23-34); and a buffer (column 6, line 32; column 3, lines 23-34), wherein the buffer records the processing data (column 5, lines 21-23) and the status of the one or more control structures (column 6, lines 33-34; column 3, lines 23-34).

Modelski does not disclose wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

Floyd, however, discloses wherein the processing data includes a lookup number (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles), wherein the lookup number identifies the number of cycles performed by the packet processor (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Floyd, in order to optimize performance during data processing operations.

9. With respect to claim 37, Modelski discloses generating processing data (column 5, lines 20-30; column 3, lines 23-34) based on one or more control structures (column 7, lines 52-55, 60-64) while revising packet data (column 3, lines 48-53, modifications of packet is interpreted to include packet header) while performing one or more lookup cycles (column 5, lines 20-30; column 3, lines 23-34); and recording the processing data (column 5, lines 21-23) and the status of the one or more control structures (column 6, lines 33-34; column 3, lines 23-34).

Modelski does not disclose wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

Floyd, however, discloses wherein the processing data includes a lookup number (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles), wherein the lookup number identifies the number of cycles performed by the packet processor (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Floyd, in order to optimize performance during data processing operations.

10. With respect to claim 53, Modelski discloses means for generating processing data (column 5, lines 20-30; column 3, lines 23-34) based on one or more control

structures (column 7, lines 52-55, 60-64) while revising packet data (column 3, lines 48-53, modifications of packet is interpreted to include packet header) while performing one or more lookup cycles (column 5, lines 20-30; column 3, lines 23-34); and means for recording the processing data (column 5, lines 21-23) and the status of the one or more control structures (column 6, lines 33-34; column 3, lines 23-34).

Modelski does not disclose wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

Floyd, however, discloses wherein the processing data includes a lookup number (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles), wherein the lookup number identifies the number of cycles performed by the packet processor (column 5, lines 49-53, a cycle counter, timer, stores the number of cycles performed by the processor; it is apparent an identifier is used to identify the number of cycles).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Floyd, in order to optimize performance during data processing operations.

11. **Claims 2, 4, 17, 19, 38, 40, 41, 52, 54, 56, 57, and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Floyd, and further in view of Brown et al. (Patent No. US 6,347,347 B1), hereinafter Brown.**

12. With respect to claims 2 and 21, Modelski and Floyd do not disclose a trigger status register, wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger.

Brown, however, discloses a trigger status register (column 4, lines 62-65 and 47-50), wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger (column 4, lines 62-65 and 47-50, address registers provides location information).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski and Floyd with the teachings of Brown, in order to achieve improved performance in systems having intelligent I/O interfaces.

13. With respect to claims 4 and 23, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses a trigger source register (column 4, lines 62-65 and 47-50, address registers provides location information), wherein the trigger source register records data identifying the location of trigger data (column 4, lines 62-65 and 47-50, address registers provides location information).

14. With respect to claim 17, 52, and 68, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses the buffer includes addresses (column 4, lines 62-65 and 47-50, address registers provides location information),

wherein the addresses consist of a processing slot and a cycle count, wherein the processing slot indicates a packet processor processing slot, wherein the cycle count indicates a packet processor cycle count (column 4, lines 62-65 and 47-50, the number of packets processed concurrently and the cycle count are variations of data that may be related to addresses).

15. With respect to claim 19, the claim is rejected for the same reason as claim 2 above. In addition, Brown discloses the packet data being revised is a datagram header (column 1, lines 49-53).

16. With respect to claim 38, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses providing information regarding the location of stored data in the buffer related to a trigger (column 4, lines 62-65 and 47-50, address registers provides location information).

17. With respect to claim 40, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses recording data identifying the location of trigger data (column 4, lines 62-65 and 47-50, address registers provides location information).

18. With respect to claim 54, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses means for providing information regarding

the location of stored data in the buffer related to a trigger (column 4, lines 62-65 and 47-50, address registers provides location information).

19. With respect to claim 56, the claim is rejected for the same reason as claims 2 and 21 above. In addition, Brown discloses means for recording data identifying the location of trigger data (column 4, lines 62-65 and 47-50, address registers provides location information).

20. **Claims 5, 41, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Floyd and further in view of Hirata (Patent No. 4,755,986)**.

21. With respect to claim 5, Modelski and Floyd do not disclose a port, wherein a packet header is combined with buffer data.

Hirata, however, discloses a port (column 2, lines 60-67), wherein a packet header (column 2, lines 60-67) is combined with buffer data (column 5, lines 38-40), and the packet header and buffer data are made available through the port (column 2, lines 60-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Hirata, in order to achieve high-speed packet processing.

22. With respect to claim 41, the claim is rejected for the same reason as claims 5 and 24 above. In addition, Hirata discloses making a packet header and buffer data available at a port (column 2, lines 60-67), wherein the packet header is combined with the buffer data (column 2, lines 60-67).

23. With respect to claim 57, the claim is rejected for the same reason as claims 5 and 24 above. In addition, Hirata discloses means for making a packet header and buffer data available at a port (column 2, lines 60-67), wherein the packet header is combined with the buffer data (column 2, lines 60-67).

24. **Claims 12-16, 47-51, and 63-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Floyd and further in view of Butler et al. (Patent No. 4,654,654), hereinafter Butler**.

25. With respect to claims 12, 47, and 63, Modelski does not disclose data stored in the buffer is provided upon the satisfaction of a trigger condition.

Butler, however, discloses data stored in the buffer is provided upon the satisfaction of a trigger condition (column 18, lines 33-46, trigger condition is based on the condition, if a match is found).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski and Floyd with the teachings of Butler, in order to minimize the extra data processing load on processors.

26. With respect to claims 13, 48, and 64, the claims are rejected for the same reason as claims 12, 32, 47, and 63 above. In addition, Butler discloses data stored in the buffer is provided to a host processor (column 5, lines 45-51) upon the satisfaction of a trigger condition from a trigger source (column 8, lines 33-46, trigger condition is based on the condition, if a match is found),wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: an ingress port, an SCT index, a CAM match address and flags, an AFH data structure, and a statistics data structure (column 8, lines 33-46, CAM is one of a group of trigger sources).

27. With respect to claims 14, 49, and 65, the claims are rejected for the same reason as claims 12, 32, 47, and 63 above. In addition, Butler discloses data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks (column 8, lines 33-52, a mask is associated with content addressable memory since finding a match for a destination address is a way of marking the data as valid).

28. With respect to claims 15, 50, and 66 the claims are rejected for the same reason as claims 12, 32, 47, and 63 above. In addition, Butler discloses data stored in the buffer includes: a first command index; an ingress port; a lookup number; a SCT index; a CAM command; a CAM key; a context pointer set; page flags; VLAN flags; L3 select flags; a VLAN identifier; a receive associated RAM derived VLAN indication; internal VPST flags; AFH derived VPST flags; a CAM match address; CAM flags; an exception

PTI; an 20 exception priority; a revised AFH data structure; and a revised statistics data structure (column 8, lines 33-46, CAM operations involve buffering data. Other data may be recorded in buffer since the functionality of a buffer is to temporarily store data).

29. With respect to claims 16, 51, and 67, the claim is rejected for the same reason as claims 12, 32, 47, and 63 above. In addition, Butler discloses the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer (column 7, lines 34-35).

30. **Claims 3, 6-11, 18, 39, 55, 42-46, and 58-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Floyd and further in view of Jotwani (Patent No. 6,148,381), hereinafter Jotwani.**

31. With respect to claim 3, Modelski and Floyd do not disclose a trigger status register, wherein the trigger status register includes a lookup count and a trigger vector, wherein the lookup count identifies data recorded in the buffer from a first cycle of the packet processor, wherein the trigger vector indicates the number of packet processor slots that met a trigger condition.

Jotwani, however, discloses a trigger status register (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of data registers and vector registers), wherein the trigger status register includes a lookup count and a trigger vector (column

8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of data registers and vector registers), wherein the lookup count identifies data recorded in the buffer from a first cycle of the packet processor (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Data registers are used to hold numeric values and accumulated values), wherein the trigger vector indicates the number of packet processor slots that met a trigger condition (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Vector registers holds data for vector processing, in which mathematical operations are performed on multiple data elements simultaneously).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski and Floyd with the teachings of Jotwani, in order to improve program execution performance.

32. With respect to claims 6, 25, 42, and 58, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor), wherein the host processor is not incorporated into

the integrated circuit (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor).

33. With respect to claims 7, 26, and 59, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is a circular buffer (column 7, lines 34-35).

34. With respect to claims 8 and 27, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a circular buffer).

35. With respect to claims 9 and 28, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is configured to operate with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor).

36. With respect to claims 10 and 29, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to

function as a mailbox for a host processor (column 8, lines 66-67; column 9, lines 1-4, mailbox is interpreted to include processor, buffers, and registers. Various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of address registers, data registers and vector registers).

37. With respect to claims 11 and 31, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is configured to operate with a host processor, wherein the mailbox is configured to be optionally programmed by the packet processor or the host processor (column 8, lines 66-67; column 9, lines 1-4, mailbox is interpreted to include processor, buffers, and registers. Various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of address registers, data registers and vector registers).

38. With respect to claim 18, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to search for data, wherein a user may specify the data searched for (column 18, lines 60-67; column 9, lines 1-6).

39. With respect to claim 22, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses a trigger status register, wherein the trigger status

register includes a trigger vector (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of vector registers), wherein the trigger vector indicates the number of packet processor slots that met a trigger condition (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Vector registers holds data for vector processing, in which mathematical operations are performed on multiple data elements simultaneously).

40. With respect to claim 39, the claim is rejected for the same reason as claim 3above. In addition, Jotwani discloses identifying data recorded in the buffer from a first cycle of the packet processor (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Data registers are used to hold numeric values and accumulated values).

41. With respect to claim 43, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses a buffer records the processing data and the status of the one or more control structures and the buffer is a circular buffer (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a circular buffer).

42. With respect to claims 44 and 60, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses a buffer records the processing data and the status of the one or more control structures (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a circular buffer), wherein the buffer is a circular buffer, and wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a circular buffer).

43. With respect to claims 45 and 61, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses a buffer records the processing data and the status of the one or more control structures (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a buffer), wherein the buffer is a circular buffer (column 7, lines 34-35), and wherein the circular buffer is configured to operate with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor).

44. With respect to claims 46 and 62, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses a buffer records the processing data and the status of the one or more control structures (column 7, lines 34-35, a buffer is used

to store various types of data, processing data and status of control structures are variations of data that can be recorded by a buffer), wherein the buffer is configured to operate with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor), wherein the buffer is configured to operate with a second processor (Fig. 1), wherein the second processor may be optionally programmed by the packet processor or the host processor (column 8, lines 66-67; column 9, lines 1-6, a microprocessor may be embedded in a larger system is interpreted as including the microprocessor being optionally programmed by another processor in the larger system).

45. With respect to claim 55, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani, however, discloses means for identifying data recorded the buffer from a first cycle of the packet processor (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Data registers are used to hold numeric values and accumulated values).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Brown with the teachings of Jotwani, in order to improve program execution performance.

46. **Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Brown.**

47. With respect to claim 21, Modelski does not disclose a trigger status register, wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger.

Brown, however, discloses a trigger status register (column 4, lines 62-65 and 47-50), wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger (column 4, lines 62-65 and 47-50, address registers provides location information).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Brown, in order to achieve improved performance in systems having intelligent I/O interfaces.

48. With respect to claim 23, the claim is rejected for the same reason as claim 21 above. In addition, Brown discloses a trigger source register (column 4, lines 62-65 and 47-50, address registers provides location information), wherein the trigger source register records data identifying the location of trigger data (column 4, lines 62-65 and 47-50, address registers provides location information).

49. **Claims 22 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Jotwani.**

50. With respect to claim 22, Modelski does not disclose a trigger status register, wherein the trigger status register includes a trigger vector, wherein the trigger vector indicates the number of packet processor slots that met a trigger condition.

Jotwani, however, discloses a trigger status register, wherein the trigger status register includes a trigger vector (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of vector registers), wherein the trigger vector indicates the number of packet processor slots that met a trigger condition (column 8, lines 66-67; column 9, lines 1-4, various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. Vector registers holds data for vector processing, in which mathematical operations are performed on multiple data elements simultaneously).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Jotwani, in order to improve program execution performance.

51. With respect to claim 25, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor), wherein the host processor is not incorporated into the

integrated circuit (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor).

52. With respect to claim 26, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses the buffer is a circular buffer (column 7, lines 34-35).

53. With respect to claim 27, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles (column 7, lines 34-35, a buffer is used to store various types of data, processing data and status of control structures are variations of data that can be recorded by a circular buffer).

54. With respect to claim 28, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses the buffer is configured to operate with a host processor (Fig. 1; column 8, lines 60-67; column 5, lines 54-57, "executes debug control software module" is interpreted as the host system containing a processor).

55. With respect to claim 29, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to function as a mailbox for a host processor (column 8, lines 66-67; column 9, lines 1-4, mailbox is

interpreted to include processor, buffers, and registers. Various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of address registers, data registers and vector registers).

56. With respect to claim 30, the claim is rejected for the same reason as claim 22 above. In addition, Jotwani discloses the system is also configured to function as a mailbox for a host processor (column 8, lines 66-67; column 9, lines 1-4, mailbox is interpreted to include processor, buffers, and registers. Various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of address registers, data registers and vector registers).

57. With respect to claim 31, the claim is rejected for the same reason as claim 3 above. In addition, Jotwani discloses the buffer is configured to operate with a host processor, wherein the mailbox is configured to be optionally programmed by the packet processor or the host processor (column 8, lines 66-67; column 9, lines 1-4, mailbox is interpreted to include processor, buffers, and registers. Various types of memory elements include registers. A processor contains several kinds of registers that can be classified according to their content. The trigger status register has the functionality of address registers, data registers and vector registers).

58. **Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Hirata.**

59. With respect to claim 24, Modelski does not disclose a port, wherein a packet header is combined with buffer data.

Hirata, however, discloses a port (column 2, lines 60-67), wherein a packet header (column 2, lines 60-67) is combined with buffer data (column 5, lines 38-40), and the packet header and buffer data are made available through the port (column 2, lines 60-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Hirata, in order to achieve high-speed packet processing.

60. **Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modelski in view of Butler.**

61. With respect to claim 32, Modelski does not disclose data stored in the buffer is provided upon the satisfaction of a trigger condition.

Butler, however, discloses data stored in the buffer is provided upon the satisfaction of a trigger condition (column 18, lines 33-46, trigger condition is based on the condition, if a match is found).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Modelski with the teachings of Butler, in order to minimize the extra data processing load on processors.

62. With respect to claim 33, the claim is rejected for the same reason as claim 32 above. In addition, Butler discloses data stored in the buffer is provided to a host processor (column 5, lines 45-51) upon the satisfaction of a trigger condition from a trigger source (column 8, lines 33-46, trigger condition is based on the condition, if a match is found), wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: a transmit modification index; packet data; and the structure of data within an address filtering header (column 8, lines 33-46, one of the trigger sources are based on the destination address which is part of packet data. Packet data is one of a group of trigger sources).

63. With respect to claim 34, the claims are rejected for the same reason as claim 32 above. In addition, Butler discloses data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks (column 8, lines 33-52, a mask is associated with content addressable memory since finding a match for a destination address is a way of marking the data as valid).

64. With respect to claim 35, the claim is rejected for the same reason as claim 32 above. In addition, Butler discloses data stored in the buffer includes: fragment CAM

data; fragment format RAM data; a fragment format RAM address; a transmit work buffer address; data from a transmit work buffer; a context pointer set; transmission engine error flags; the current packet size adjustment; the amount of original egress packet data inside the transmit work buffer; the current packet pointer; the last sequence flag, an address rewind flag; a slush flag; a processor sequence number; and a transmit modification command (column 8, lines 33-46, CAM operations involve buffering data. Other data may be recorded in buffer since the functionality of a buffer is to temporarily store data).

65. With respect to claim 36, the claim is rejected for the same reason as claim 32 above. In addition, Butler discloses the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer (column 7, lines 34-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TREVILLIAN HIGHTER whose telephone number is (571)270-3806. The examiner can normally be reached on Monday-Friday 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571)272-3984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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THH 4/8/2008

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